ISSN 2349-7815

International Journal of Recent Research in Electrical and Electronics Engineering (IJRREEE)
Vol. 2, Issue 2, pp: (6-10), Month: April 2015 - June 2015, Available at: www.paperpublications.org

Design and Optimization of GDI Based 1-bit Comparator using Reverse Logic

[1]Sukhdeep Kaur, [2]Hardeep kaur, [3]Er. Poonam Rani

[1,2]Student of M-Tech (ECE), [3]Assistant Professor Dept. Of ECE, Baba Farid College of Engineering and Technology, Bathinda, Punjab, India

Abstract: **Today's electronics world competing with low power and less area of digital combinatorial circuits. A reverse logic gates are designed to reduce transistor count, area and power dissipation of digital comparator circuit .The GDI module based design of 1-bit reverse comparator is proposed using reversible L and M gates and simulation done on TANNER EDA tool. L and M reverse logic gates downscaled using constant electrical field scaling to design proposed 1-bit reverse comparator circuit using 180nm technology. At 5V supply voltage power dissipation analyzed 0.162mW that is 10% improvement as compared to CMOS circuit design.**

Keywords**: Reverse Logic, L and M gate, Power dissipation, Gate Diffusion Input.**

1. INTRODUCTION

In electronics era optimization of technology of a circuit design is main issue to be concerned. The fundamental requirement of digital circuit design to reduce power reduction at the cost of low supply voltage. The keen efforts done by using reverse logic gates [1].The channel length and width of transistor PMOS and NMOS is important parameter for deduction in power dissipation and Garbage outputs, constant outputs replacing with reversible inputs.

2. COMPARATOR

The basic comparator to compare two analog signals or two digital signals but outputs a digital signal binary logic '0' or '1'.For exact and fast conversion, digital comparator is implemented in ADC(analog to digital convertor) to increase battery life. Voltage resolution too sensitive 18mV to 50mV.The comparison with CMOS reverse comparator design problem of area optimization solved by large scalar quantity that is main aim of reverse logic style.

Truth table of 1-bit comparator circuit

input	input	output	output	output
A	B	p(A=B)	q(A>B)	r(A<B)
0	0	1	0	0
0	1	0	0	1
1	0	0	1	0
1	1	1	1	0

ISSN 2349-7815

International Journal of Recent Research in Electrical and Electronics Engineering (IJRREEE)
Vol. 2, Issue 2, pp: (6-10), Month: April 2015 - June 2015, Available at: www.paperpublications.org

3. REVERSE LOGIC GATE

Basically this circuit is one-to-one mapping that shows only one specific output logic according to particular input logic. Some important reversible logic gates are Feynman gate, Fredkin gate, Toffoli gate, Press gate, R-gate, TR gate [1]. But L and M reversible gates are most evaluated to reduce transistor count, merely one garbage input (G) is introduced. Two reversible inputs and constant inputs (C) as shown.

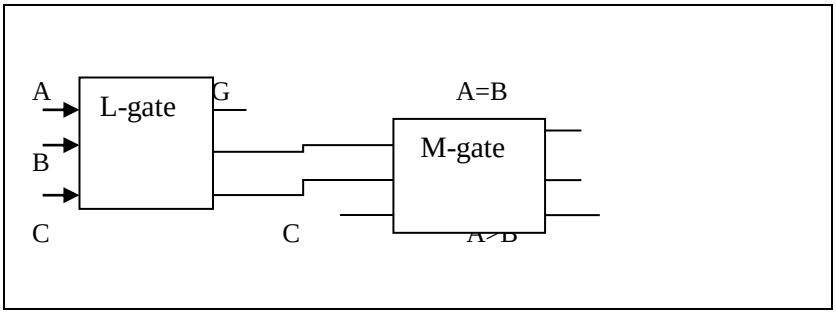


Fig.1.1 Block diagram of reversible 1-bit comparator

Evaluation on tanner tool EDA the circuit diagrams of both L and M gates using GDI cells. In circuit diagrams, A and B input bits, C is constant input 'G' is garbage input(only one).Two reversible inputs showing L-gate .In this paper a new approach of digital combinatorial circuit 1-bit reverse comparator is designed using GDI(Gate Diffusion Input) technique.

4. GATE DIFFUSION INPUT

At first sight circuit realization of Basic GDI cell reminds us CMOS inverter, having three inputs P,N and G as shown.

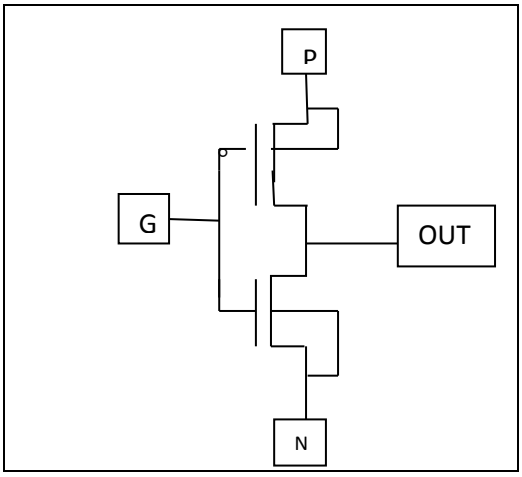


Fig 1.2 Basic GDI cell

(1)As in inverter vdd replaced with input of outer diffusion node of pMOS transistor (P).

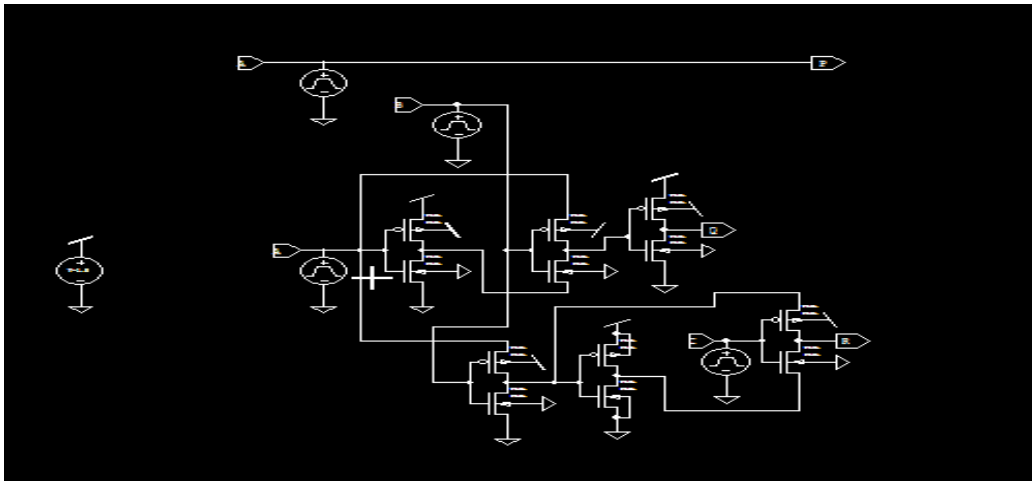
(2)G input (common gate input of both pMOS and nMOS.

(3)GND (ground) of inverter circuit not connected to source of nMOS, instead input (N) to outer diffusion node of nMOS transistor.

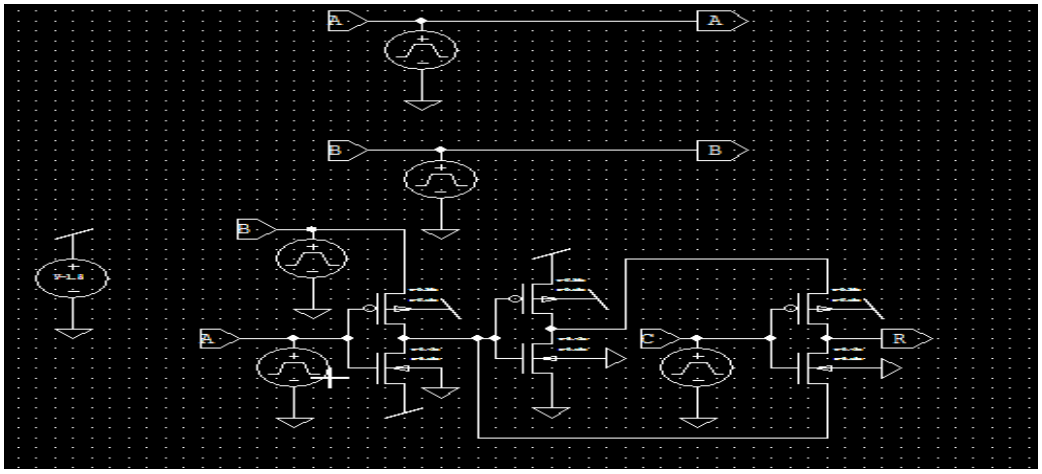
Bulks of nMOS and pMOS connected to N and P respectively that biased it with CMOS inverter.Our design to optimization of area and power efficiency by altering the channel-length of both pMOS and nMOS, widths of pMOS and nMOS [5].

ISSN 2349-7815

International Journal of Recent Research in Electrical and Electronics Engineering (IJRREEE)
Vol. 2, Issue 2, pp: (6-10), Month: April 2015 - June 2015, Available at: www.paperpublications.org



Reverse Logic M-gate using GDI module



Reverse Logic L-gate using GDI module

In order to accommodate proposed design dissipate less power constant electric field scaling done letting other parameters as it in previous improved design. Area (A) of CMOS inverter is product of channel-length (L) and width (W) of a pMOS and nMOS device [7]. It reduced as number of transistors decreased in circuit implementation. Total minimum area can be achieved by scaling gate area (Ag) for W and L (for nMOS and pMOS devices) that is function of transistor count (N).As usage of inverter reminds GDI cell,

$$A = Ao(Wp * Lp + Wn * Wn)$$

Ao is constant of proportionality, Wp, Wn, Lp, Ln channel widths and lengths of pMOS and nMOS respectively. Determination of previous improved CMOS circuit design implement 50 transistors and GDI technique implement only 18 transistors [1].

5. POWER CONSUMPTION IN CMOS CIRCUITS

Mainly power dissipated when operation is dynamic, static power dissipation too small at this stage not considered [2]. Total power dissipation (P) defined as

$$P = P(static) + P(dynamic) + p(short\ circuit)$$

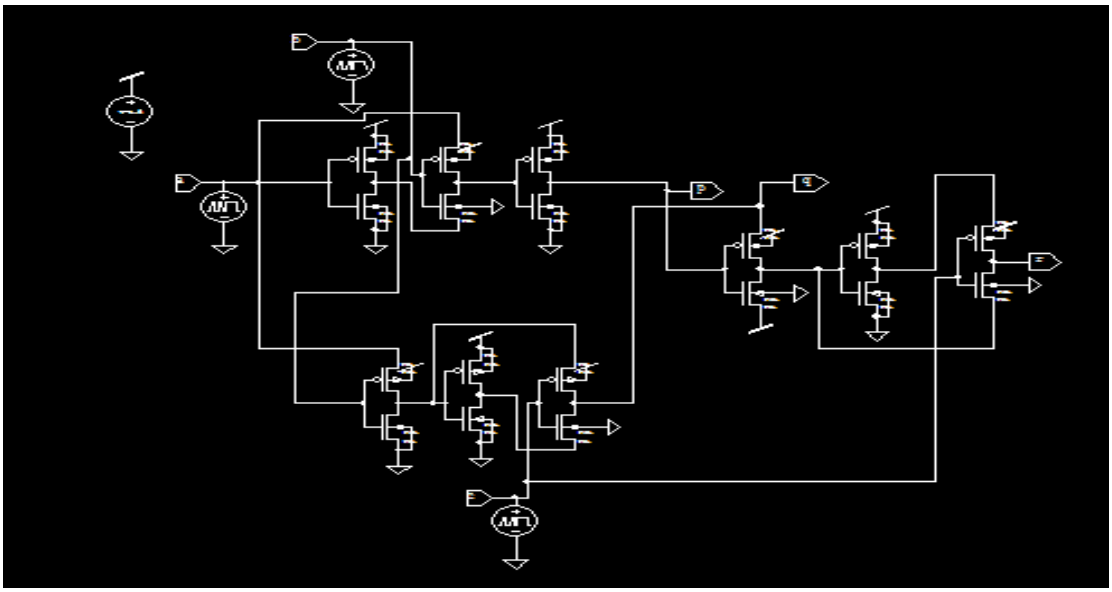
Where P (static) is power dissipation due to reverse biasing of drain and bulk a reverse leakage current drawn from supply voltage (Dynamic) it is main component of total power dissipation due to load capacitance, power supply voltage drawn, frequency used and switching activities (short circuit) the time both transistors on a direct path between vdd and ground formed short circuit power dissipation takes place [3].

ISSN 2349-7815

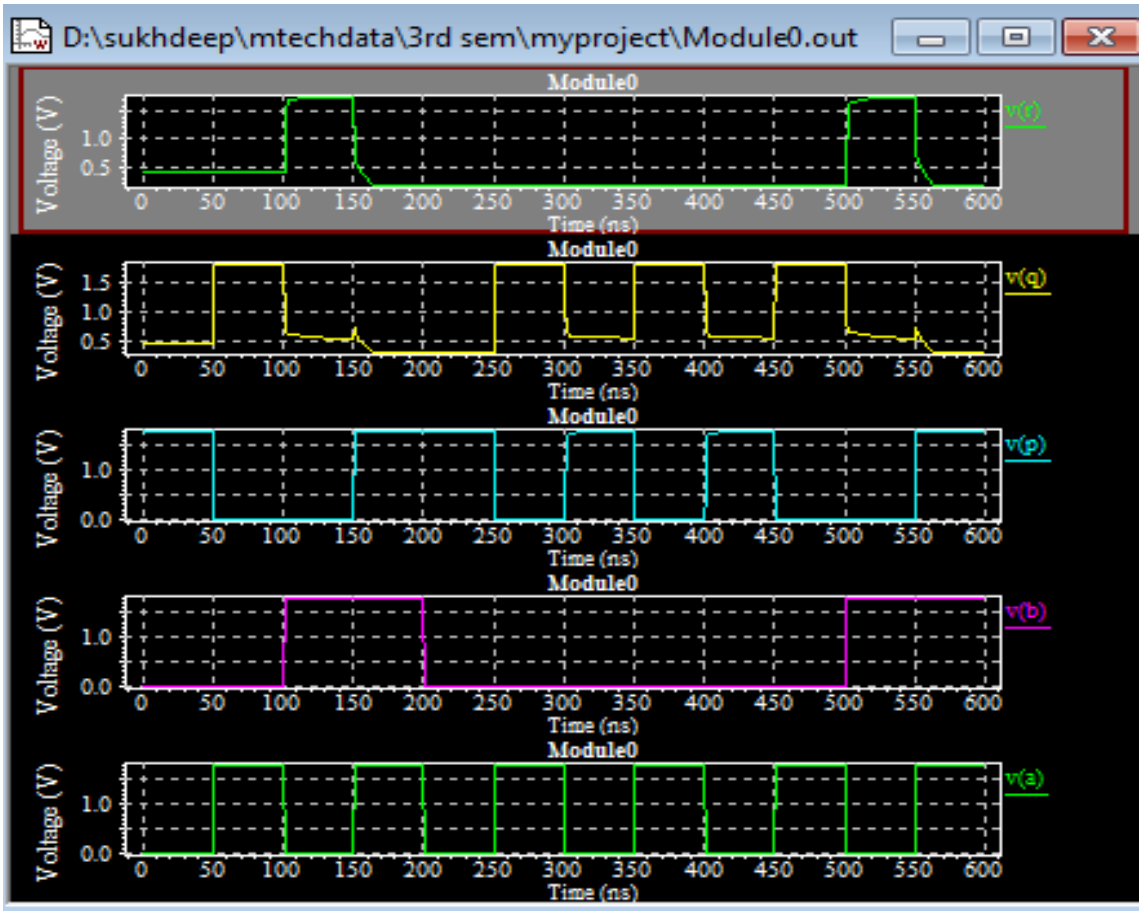
International Journal of Recent Research in Electrical and Electronics Engineering (IJRREEE)
Vol. 2, Issue 2, pp: (6-10), Month: April 2015 - June 2015, Available at: www.paperpublications.org

6. RESULTS

The simulation performed using width of nMOS 0.36um and width of pMOS 0.72um with channel length 0.18um. At 5V supply voltage CMOS using 50 transistors 1-bit reverse comparator circuit is implemented [1].In this paper, constant electric field scaling is done.



Schematic of Reverse Logic 1-bit comparator circuit



Input and Output waveforms of proposed Reverse Logic 1-bit comparator circuit.

Table.1 Performance parameters of comparator

Proposed design using	Transistor Count	Channel Length (um)	Power Dissipation (mW)	Width of pMOS (um)	Width nMOS (um)	Voltage Applied (V)
GDI	18	0.18	0.162	0.72	0.36	5
CMOS	50	0.18	1.715	2	1	5

7. CONCLUSIONS AND FUTURE WORK

In order to design power efficient and area optimized 1-bit reverse comparator area and power factors are significantly decreased as contrast to CMOS at 5V supply voltage. As schematic of circuit design depicted only 18 transistors used to implement proposed circuit design using GDI technology. Transistor count is highly optimized as compare to CMOS that needs 50 transistors to implement same design style. Future scope of research put efforts on implementation of higher order design of n-bit reverse comparators for power efficient ADC's.

REFERENCES

[1] Madhisha basha ,V.N. Lakhsmana kumar,"transistror implementation of reversible comparator circuit using low power techniaque" International journal of computer science and information technologies vol. 3(3),page no. 4447-4452,2012.

[2] Arkadiy Morgenshtein, Alexander fish and Israel A. Wagner "Gate-Diffusion input (GDI): A power efficient method for digital combinatorial circuits" IEEE Transactions on very large scale integration (VLSI) systems, vol.10, no. 5, October, 2002.

[3] Pooja Verma ,Racha Manchnda "Review of GDI techniques for low power digital circuits" International General of Emerging Technology and Advance Engineering,volume 4,issue 2,feburary,2014.

[4] A.N. Nagamani , H V jayashree ,H R bhagyalakshmi "Noval low power reverse comparator design using reversible logic gates" Indian journal of computer science and engineering vol.2 No.4 ,aug sept 2011.

[5] Y.Syamala, K shrilaksmi and N .Somasekhar Varma "design of low power CMOS circuits using Gate Diffusion Input (GDI) Technique" International general of VLSI design & communication systems,vol.4,No.5,October 2013.

[6] Eric R. Menendez Dumezie K. Maduike, Rajesh Garg, Sunil P khatri "CMOS comparators for High-speed and low power application" 1-4244-9707-X/06/$20.002006 IEEE.

[7] Douglous A. Pucknell, Kamran Eshraghian, "basic VLSI design third edition,2013.

[8] Jing Zhu ,Weifeng Sun, Hui chen , and Shengli Lu, "Investigation on Electrical Degradation of high temperature Reverse Bias stress ,IEEE transactions o device and materials reliability ,vol.14,No. 2,june 2014.